ABSTRACT OF THE DISCLOSURE

In a command input circuit: m command acquisition units are provided corresponding to first to mth commands, respectively, where m is an integer greater than one; a clock signal supplying unit supplies n clock signals respectively having different phases to the m command acquisition units, where n is an integer greater than one; and a command input unit receives said first to mth commands, and supplies the first to mth commands to the m command acquisition units. Each of the m command acquisition units acquire one of the first to mth commands corresponding to the command acquisition unit in response to one of m edges of the n clock signals corresponding to the one of the first to mth commands. The processing unit performs processing in accordance with the first to mth commands.